LISTING OF THE CLAIMS

This listing of claims replaces all prior versions and listing of claims in the present application:

1-11. (Cancelled)

12. (Currently Amended) A clock and data recovery circuit comprising:

a phase synchronization loop including:

an oscillator outputting a clock signal, a ~~the oscillation~~ frequency of which is variably controlled based on a control signal supplied thereto;

a first phase detector detecting a phase difference between said clock signal output from said oscillator and a received data signal; and

a first integrator integrating an output from said first phase detector to supply an integrated signal to said oscillator as said control signal~~, said phase synchronization loop performing phase synchronization of a recovered clock signal, output from said oscillator, with an input data signal~~;

a discriminator circuit, responsive to a discrimination clock signal, ~~for~~ discriminating said ~~input~~ received data signal and outputting ~~the~~ a discriminated data signal;

a second phase detector circuit ~~for~~ detecting ~~the~~ a phase difference between ~~an output~~ said discriminated data signal, discriminated and output by said discriminator circuit, and said ~~input~~ received data signal;

a second integrator integrating a comparison result output from said second phase detector circuit; and

a phase shift circuit ~~for~~ shifting ~~the~~ a phase of ~~the~~ said ~~recovered~~ clock signal, output from said oscillator, based on ~~a comparison result output from said phase detector circuit~~ an integrated signal from second integrator, to produce ~~the~~ said discrimination clock signal[[~~;~~]]

~~the discrimination clock signal, output from said phase shift circuit, being~~ supplied ~~as said clock signal for discrimination~~ to said discriminator circuit,

wherein ~~the~~ said discriminator circuit, ~~the~~ said second phase detector circuit, said second integrator and ~~the~~ said phase shift circuit comprise a feedback loop separate from ~~the~~ said phase synchronization loop.

13. (Currently Amended) A clock and data recovery circuit comprising:

a first feedback loop at least including:

a voltage-controlled oscillator circuit varying an oscillation frequency based on a control signal voltage supplied thereto;

a first phase detector circuit ~~for detecting~~ supplied with a clock signal output from said voltage-controlled oscillator circuit and with a received data signal to detect ~~the~~ a phase difference between ~~a recovered~~ said clock signal and ~~a~~ said received data signal; and

a first integrator circuit integrating an output of said first phase detector circuit to supply an integrated signal to said voltage-controlled oscillator circuit as said control signal voltage; and

a second feedback loop including:

a discriminator circuit supplied with said received data signal, said discriminator circuit discriminating said received data signal, responsive to a discrimination clock signal supplied thereto; and

a second phase detector circuit ~~for detecting the phase difference between an output data signal, discriminated and output by said discriminator circuit, and said received data signal, the second feedback loop being separate from the first feedback loop~~ supplied with an output data signal discriminated and output by said discriminator circuit and with said received data signal to detect a phase difference between said two signals supplied; and

a second integrator circuit integrating an output of said second phase detector circuit; and

a phase shift circuit supplied with said clock signal output from said voltage-controlled oscillator circuit and with an integrated signal output from said second integrator circuit, said phase shift circuit shifting a phase of said clock signal supplied in accordance with said integrated signal output from said second integrator circuit, to output a resulting clock signal;

said clock signal output from said phase shift circuit being supplied to said discriminator circuit, as said discrimination clock signal and being output as an output clock signal.

~~a clock recovery circuit for being controlled by said first and second feedback loops to output the recovered clock signal;~~

~~the recovered clock signal output from said clock recovery circuit being supplied as a discrimination clock signal for discrimination by said discriminator circuit.~~

14. (Cancelled)

15. (Currently Amended) A clock and data recovery circuit comprising:

a first feedback loop including: ~~a first phase detector circuit for detecting the phase difference between an input reference clock signal and a recovered clock signal~~

a voltage-controlled oscillator circuit varying an oscillation frequency based on a control signal voltage supplied thereto;

a first phase detector circuit receiving a clock signal output from said voltage-controlled oscillator circuit and a reference clock signal to detect a phase difference therebetween; and

a first integrator circuit integrating an output of said first phase detector circuit to supply an integrated signal to said voltage-controlled oscillator circuit as a control signal voltage; and

a second feedback loop including:

a discriminator circuit supplied with a received data signal, said discriminator circuit discriminating said received data signal, responsive to a discrimination clock signal supplied thereto; ~~and~~

a second phase detector circuit supplied with an output data signal discriminated and output by said discriminator circuit and with said received data signal to detect a phase difference between said two signals supplied ~~for detecting the phase difference between an output data signal discriminated and output by said discriminator circuit and said received data signal, the second feedback loop being separate from the first feedback loop;~~

a second integrator circuit integrating an output of said second phase detector circuit; and

a phase shift circuit supplied with said clock signal output from said voltage-controlled oscillator circuit and with an integrated signal output from said second integrator circuit, said phase shift circuit shifting a phase of said clock signal supplied in accordance with said integrated signal output from said second integrator circuit, to output a resulting clock signal;

said clock signal output from said phase shift circuit being supplied to said discriminator circuit, as said discrimination clock signal and being output as an output clock signal

~~a clock for discrimination of said discriminator circuit being supplied from a clock recovery circuit controlled by said first and second feedback loops~~.

16-17. (Cancelled)

18. (Currently Amended) The clock and data recovery circuit according to claim 15, wherein said first feedback loop includes:

a selection circuit supplied with [[~~a~~]] said reference clock signal and with said received data signal to output one of ~~the~~ said signals, based on a selection control signal supplied thereto;

~~a voltage-controlled oscillator circuit for varying the oscillation frequency based on an input control signal voltage;~~ and wherein

[[~~a~~]] said first phase detector circuit is supplied with ~~the~~ said ~~recovered~~ clock signal output from said voltage-controlled oscillator circuit and with ~~the~~ a signal output from said selection circuit to detect ~~the~~ a phase difference therebetween~~; and~~

~~a first integrator circuit for integrating an output of said first phase detector circuit to supply the resulting output voltage as a control signal voltage to said voltage-controlled oscillator circuit; and wherein~~

~~said second feedback loop includes:~~

~~a second integrator circuit for providing an integrated output of said second phase detector circuit; and~~

~~a phase shift circuit supplied with the recovered clock signal output from said voltage-controlled oscillator circuit and with the integrated output of said second integrator circuit to shift the phase of the input clock signal in accordance with said integrated output supplied to output the resulting discrimination clock signal;~~

~~the discrimination clock signal output from said phase shift circuit being supplied to said discriminator circuit as a signal for discrimination and being output as an output clock signal~~.

19. (Currently Amended) The clock and data recovery circuit according to claim 13, wherein ~~the~~ a time constant of said first feedback loop is selected to be larger than ~~the~~ a time constant of said second feedback loop.

20. (Currently Amended) The clock and data recovery circuit according to claim 15, wherein ~~the~~ a time constant of said first feedback loop is selected to be larger than ~~the~~ a time constant of said second feedback loop.

21-25. (Cancelled)

26. (Currently Amended) The clock and data recovery circuit according to claim 13 [[14]], wherein said first phase detector circuit compares ~~the~~ a phase of said received data signal supplied to a first input end thereof with that of said ~~recovered~~ clock signal supplied to a second input end thereof from said voltage-controlled oscillator circuit to output a comparison result at an output end thereof;

said first integrator circuit is supplied with an output signal from said first phase detector circuit to integrate the signal supplied;

~~said clock recovery circuit includes a~~ said voltage-controlled oscillator circuit is supplied with an output signal of said first integrator circuit at an input end thereof to change ~~the~~ said oscillation frequency based on an output signal from said first integrator circuit to output ~~the~~ a resulting ~~recovered~~ clock signal at an output end thereof;

said ~~recovered~~ clock signal, output from said ~~clock recovery~~ voltage-controlled oscillator circuit ~~being~~ is fed back to a second input end of said first phase detector circuit,[[;]]

said discriminator circuit is supplied with said received data signal at a data input end thereof to discriminate said received data signal based on ~~the~~ said discrimination clock signal supplied to a clock input terminal thereof to output a data signal at an output end thereof;

said second phase detector circuit compares ~~the~~ a phase of said output data signal supplied to a first input end thereof from said discriminator circuit with that of said received data signal supplied to a second input end thereof to output a comparison result at an output end thereof;

said second integrator circuit is supplied with an output signal from said second phase detector circuit to integrate ~~the~~ said signal supplied; ~~and~~

[[~~a~~]] said phase shift circuit is supplied with said ~~recovered~~ clock signal output from said ~~clock recovery~~ voltage-controlled oscillator circuit at an input end thereof and with an integrated ~~output~~ signal output from said second integrator circuit at a control signal input end thereof to shift ~~the~~ a phase of ~~the~~ said ~~recovered~~ clock signal output from said ~~clock recovery~~ voltage-controlled oscillator circuit, based on said integrated ~~output~~ signal output from said second integrator circuit, to output ~~the~~ a resulting discrimination clock signal at an output end thereof; and

~~the~~ said discrimination clock signal output from said phase shift circuit ~~being~~ is supplied to said discriminator circuit ~~as said clock signal for discrimination~~.